

FIG.1

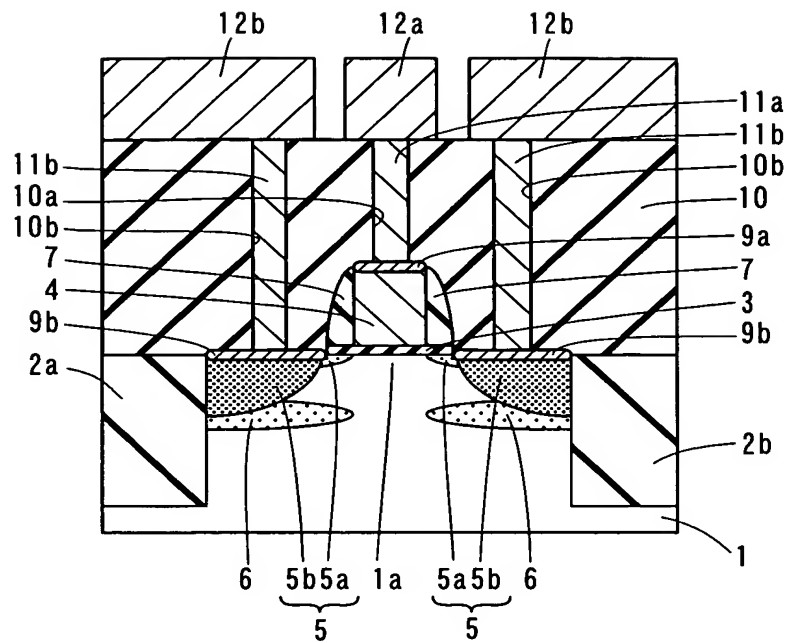


FIG.2

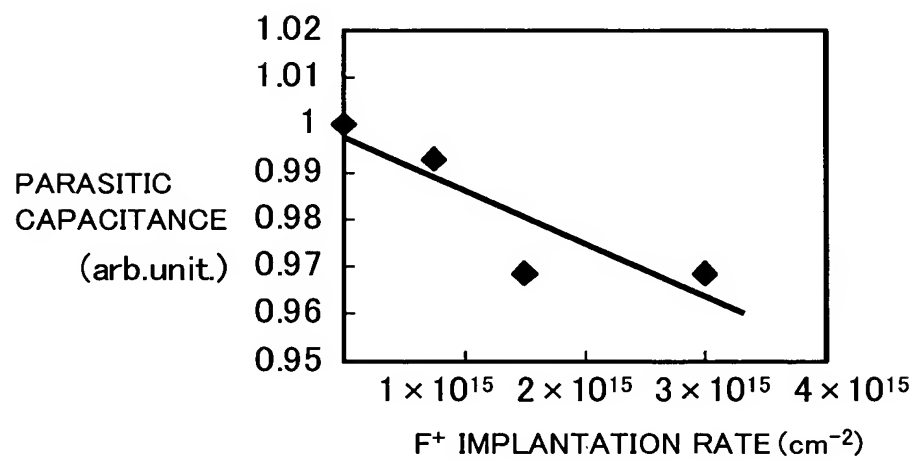


FIG.3

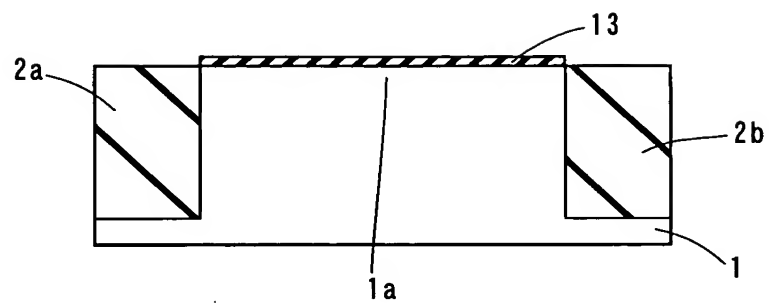


FIG.4

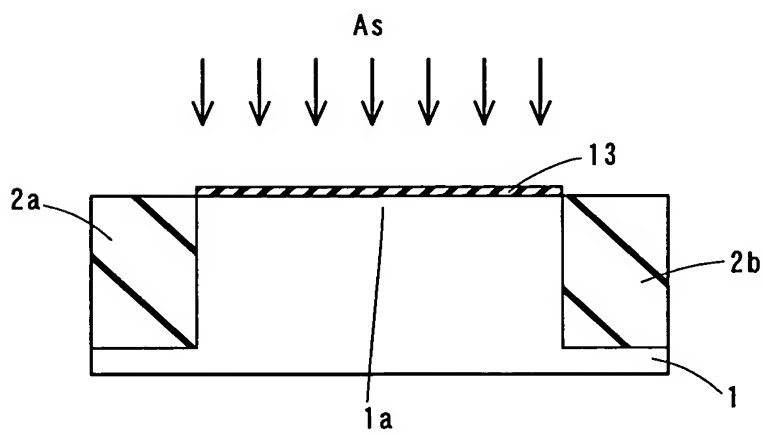


FIG.5

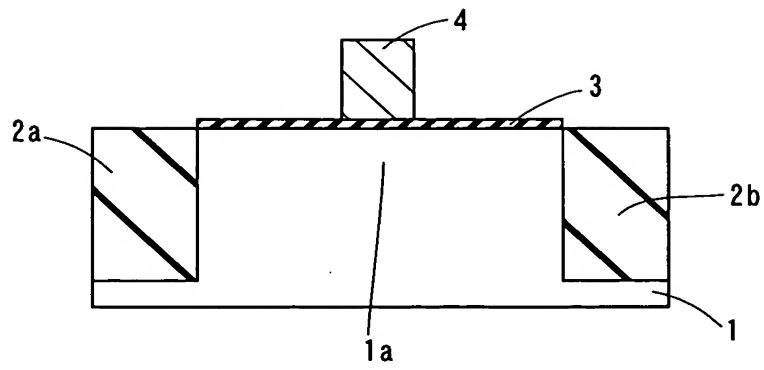


FIG.6

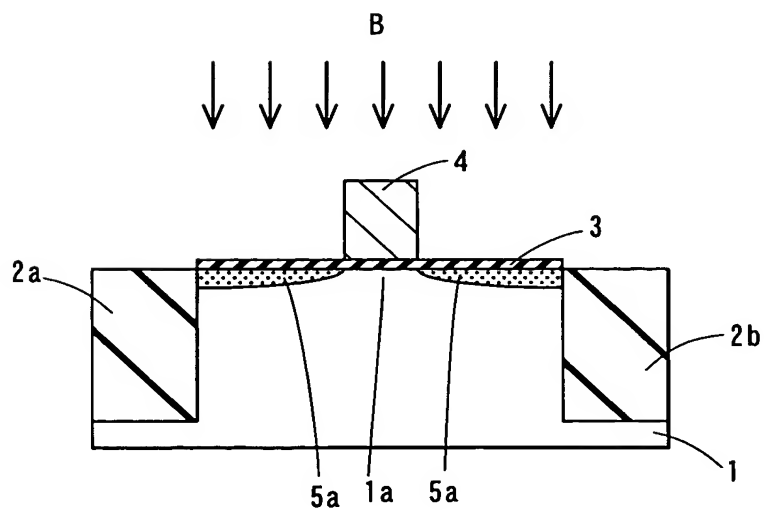


FIG.7

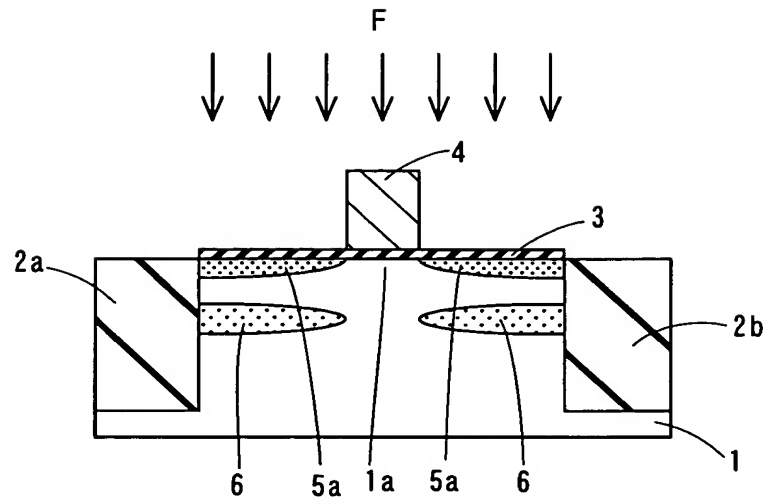


FIG.8

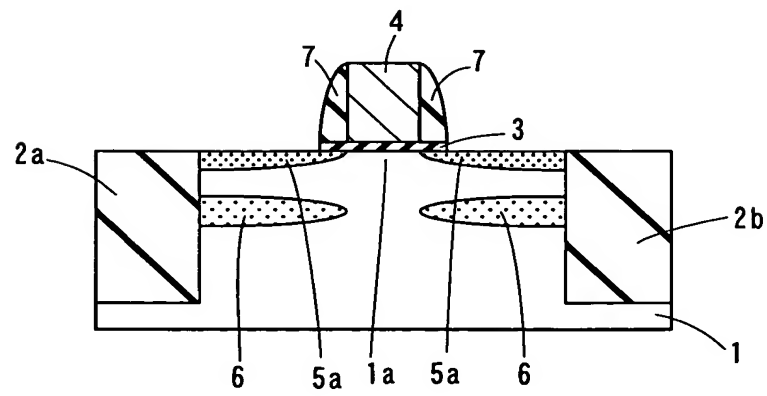


FIG.9

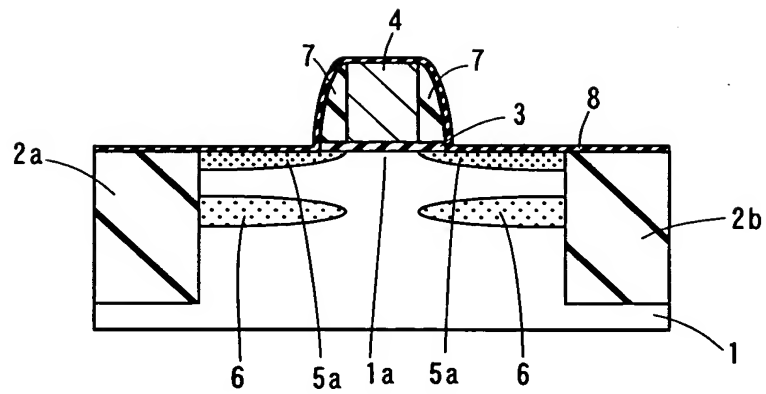
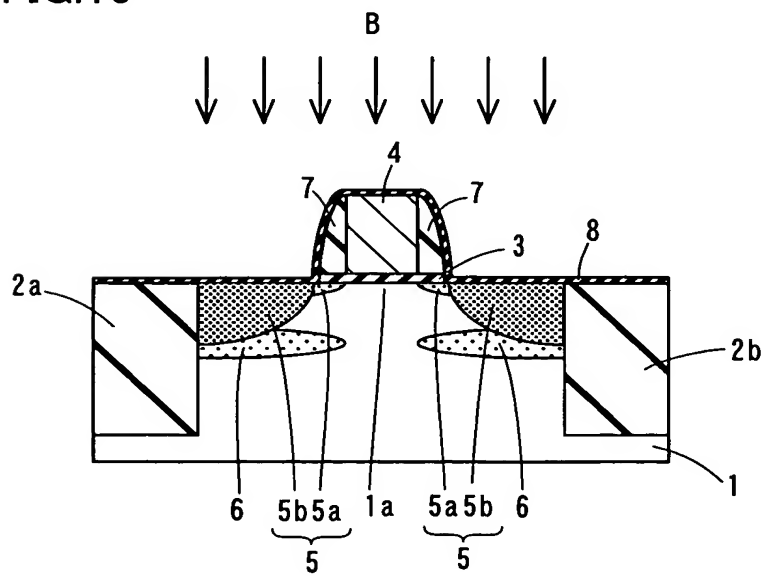


FIG.10



A cross-sectional diagram of a semiconductor device. A central substrate (1) has two regions (2a, 2b) on either side. Between them are two p-n junction structures (5). Each structure consists of a base layer (6), a middle layer (5a), and a top layer (5b). The top layers (5a, 5b) are separated by a gap (9a) and connected by a bridge (7). The entire assembly is covered by a protective layer (3). Labels 1, 2a, 2b, 3, 4, 5, 5a, 5b, 6, 7, 8, 9a, and 9b identify various components and features.

A line graph showing the relationship between the F⁺ implantation rate and the threshold voltage. The x-axis represents the F⁺ implantation rate in cm⁻², ranging from 0 to 4 × 10¹⁵. The y-axis represents the threshold voltage in Volts (V), ranging from 0 to -0.8. Three data points are plotted, showing a constant threshold voltage of approximately -0.55 V for implantation rates up to 3 × 10¹⁵ cm⁻².

F ⁺ Implantation Rate (cm ⁻²)	Threshold Voltage (V)
0	-0.55
1.5 × 10 ¹⁵	-0.55
3 × 10 ¹⁵	-0.55

[illegible]

FIG.17

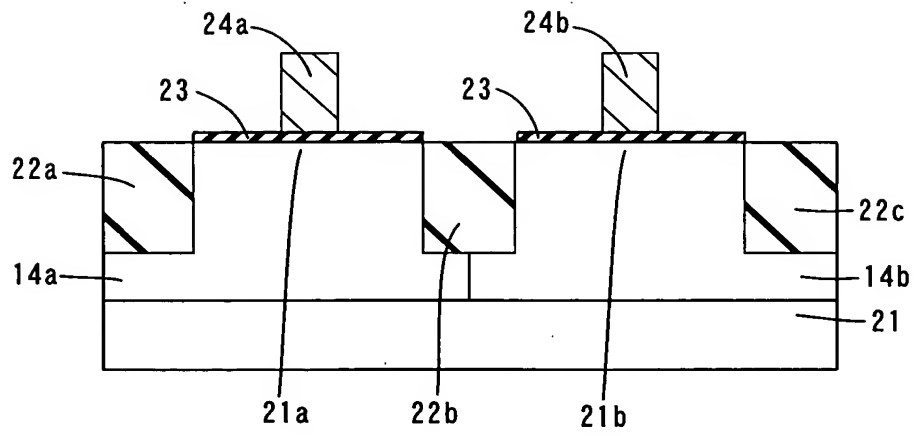


FIG.18

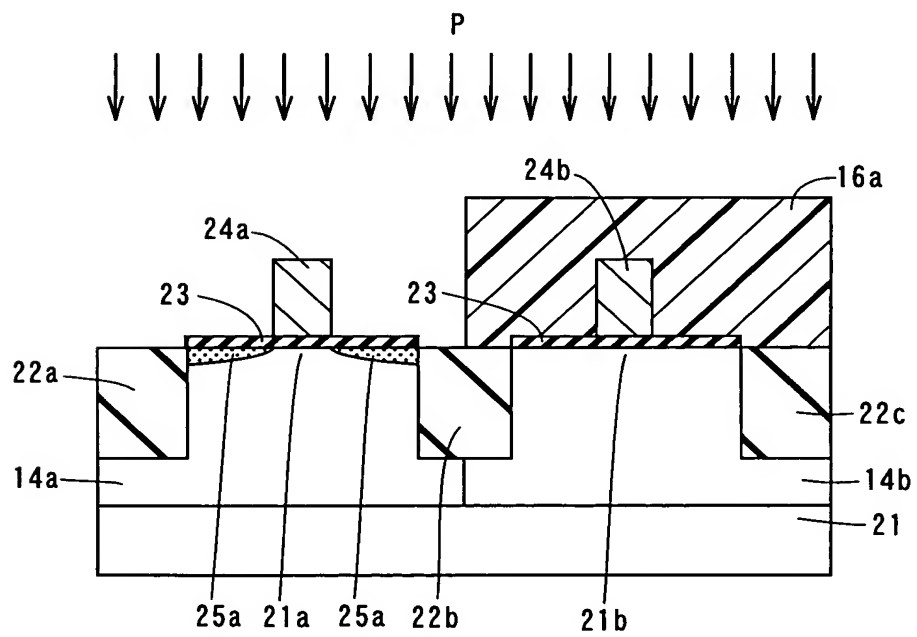


FIG.19

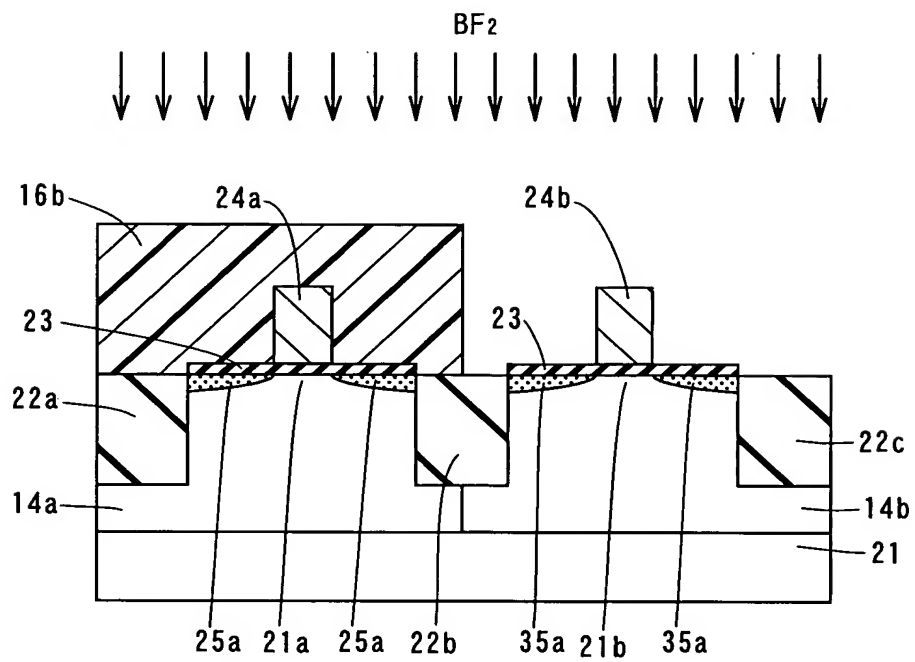


FIG.20

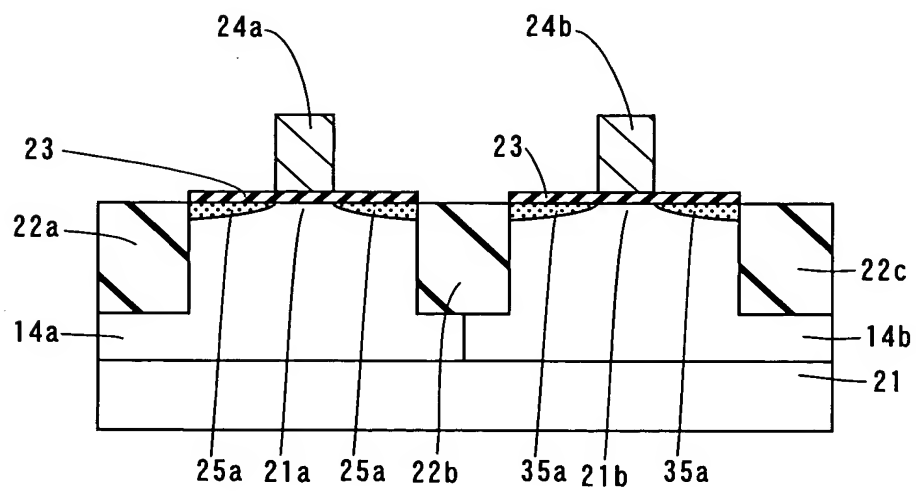


FIG.21

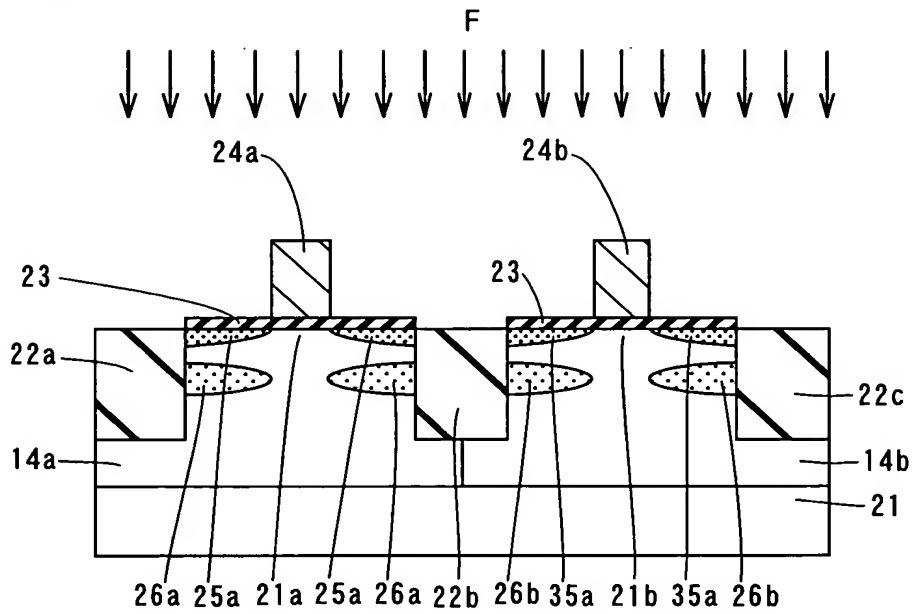
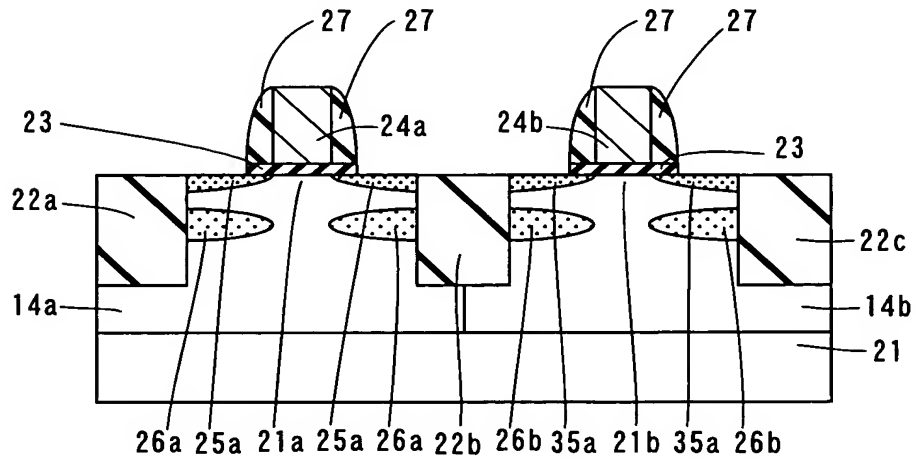


FIG.22



This cross-sectional view shows a semiconductor device with two active regions. A substrate 21 is at the base. Above it is a layer 14b. On top of 14b are two rectangular regions 14a. Within each 14a is a layer 22a. Above 22a is a layer 23. On top of 23 are two dome-shaped structures 27. Between the domes and on the sides are regions 24a and 24b. Below the substrate 21, there are labels 26a, 25a, 21a, 25a, 26a, 22b, 26b, 35a, 21b, 35a, 26b, which likely correspond to different layers or regions in the substrate or underlying structure.

A cross-sectional view of a semiconductor device. At the top, a layer labeled 'As' is shown with downward-pointing arrows indicating ion implantation. Below this is a gate stack consisting of a gate dielectric (23) and a gate electrode (27). The gate electrode is divided into two regions, 24a and 24b. The device features two transistors. The first transistor has a channel region (21a) and source/drain regions (25a, 25b). The second transistor has a channel region (21b) and source/drain regions (25a, 25b). The source/drain regions are formed by a combination of a base layer (26a, 26b) and a top layer (22a, 22b). The device is built on a substrate (21). Other labels include 14a, 14b, 17a, 17b, 22c, 23, 24a, 24b, 25a, 25b, 26a, 26b, 27, and 28.

FIG.25

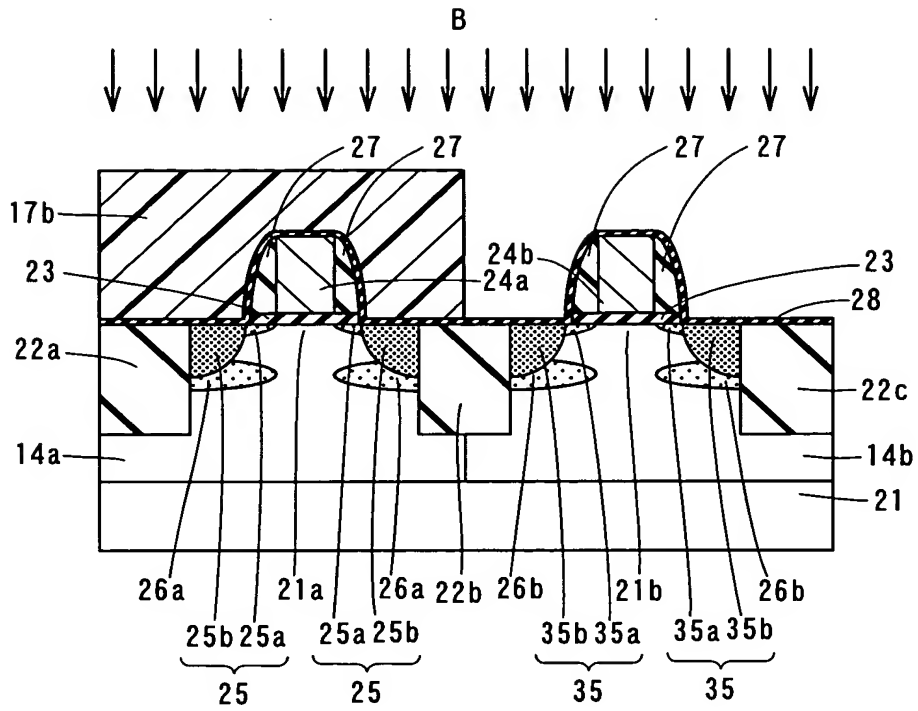


FIG.26

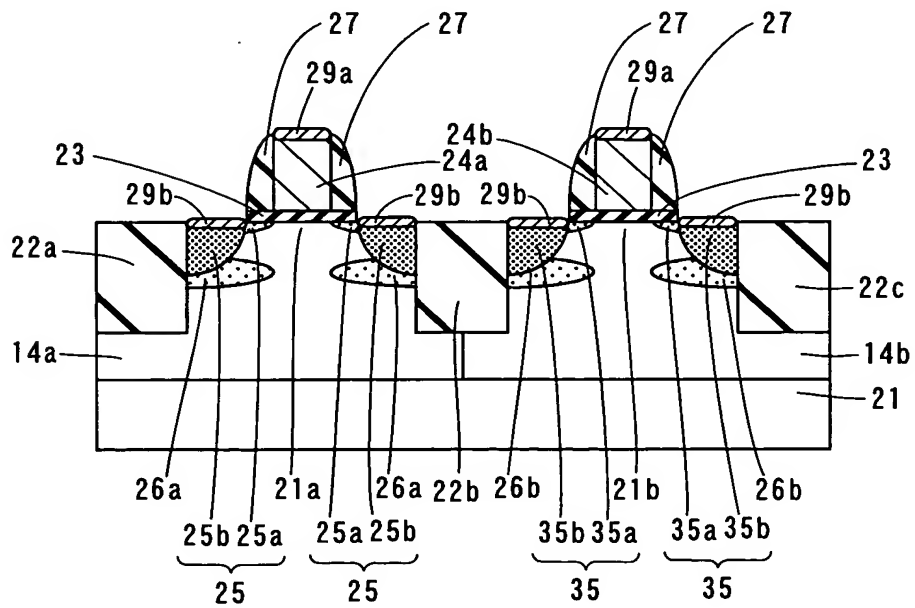


FIG.27

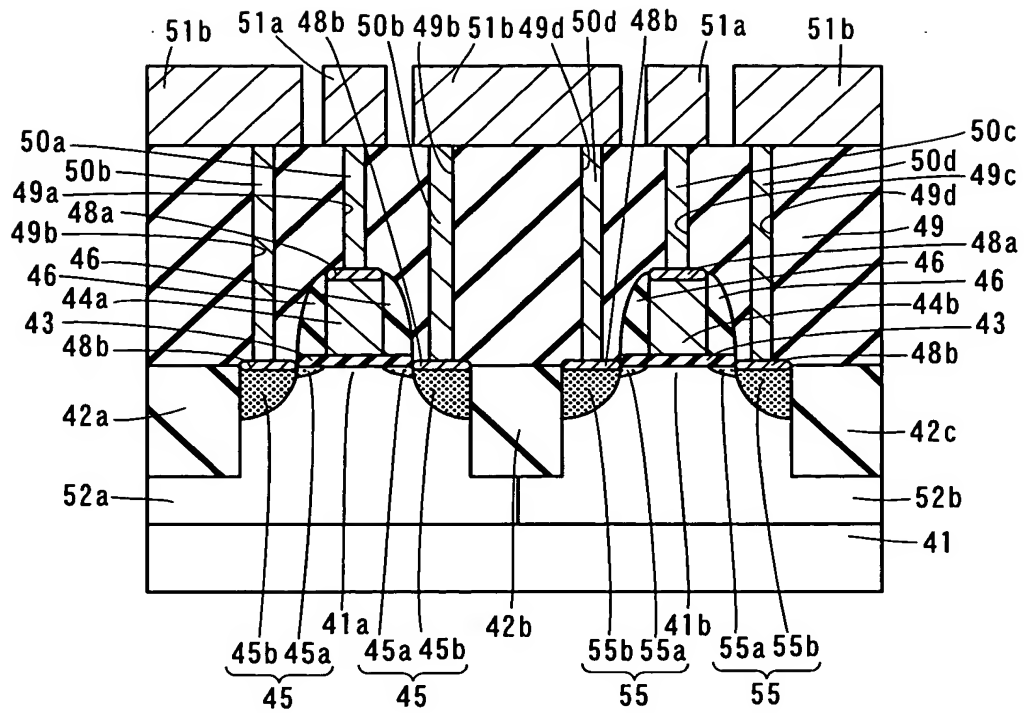


FIG.28

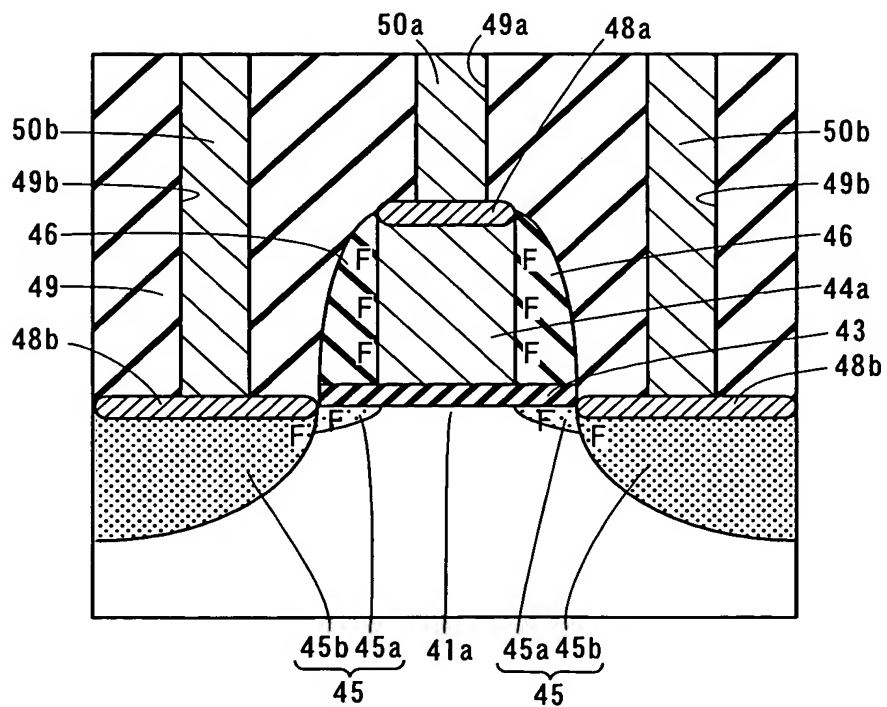


FIG.29

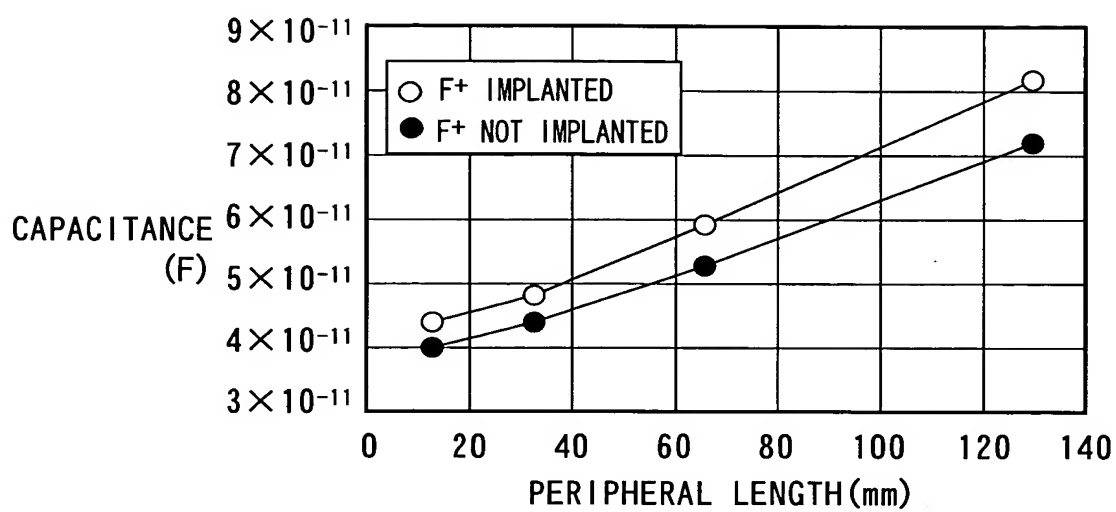
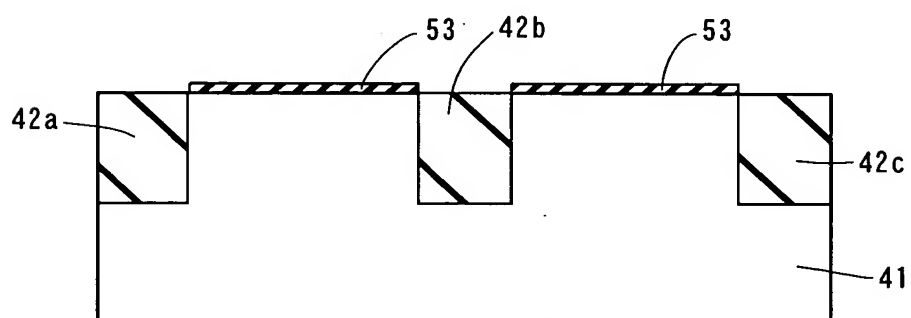


FIG.30



[illegible]

FIG.33

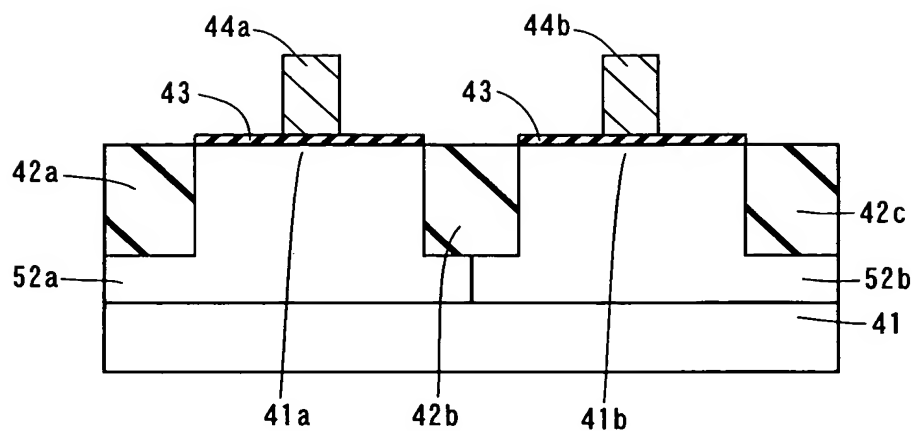


FIG.34

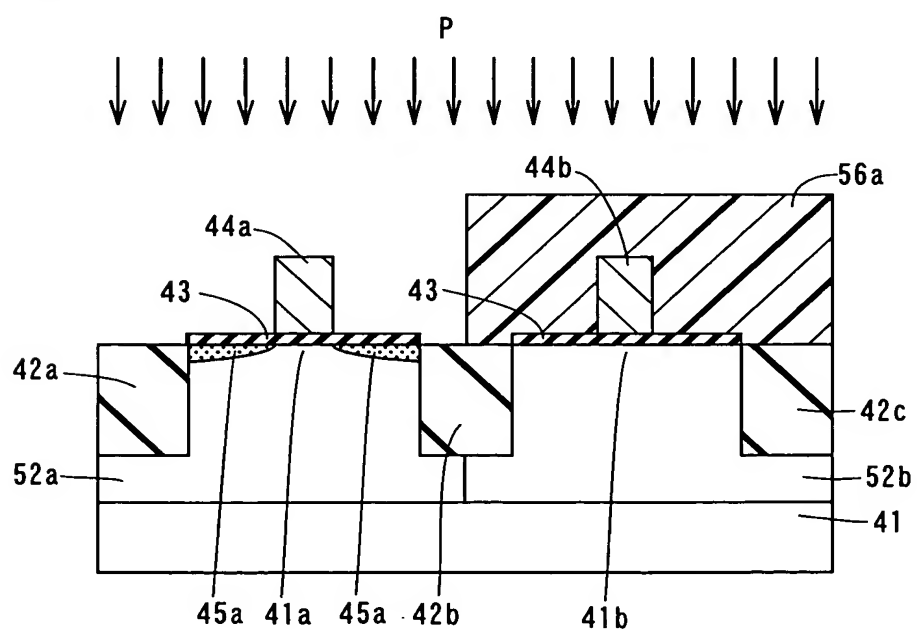


FIG.35

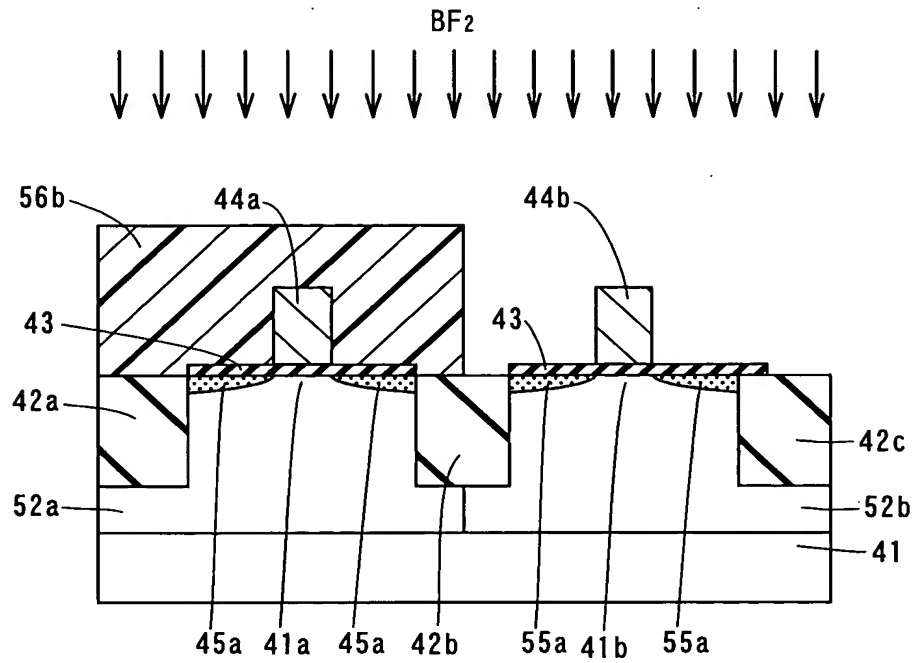


FIG.36

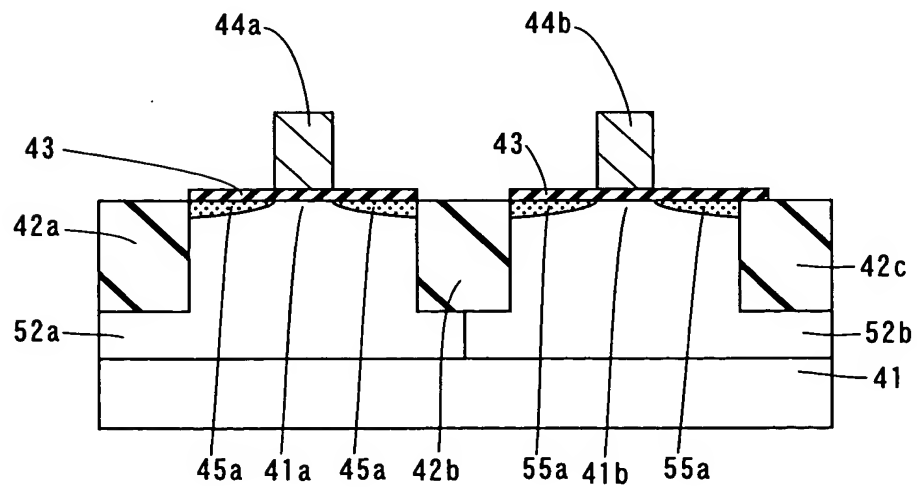


FIG.37

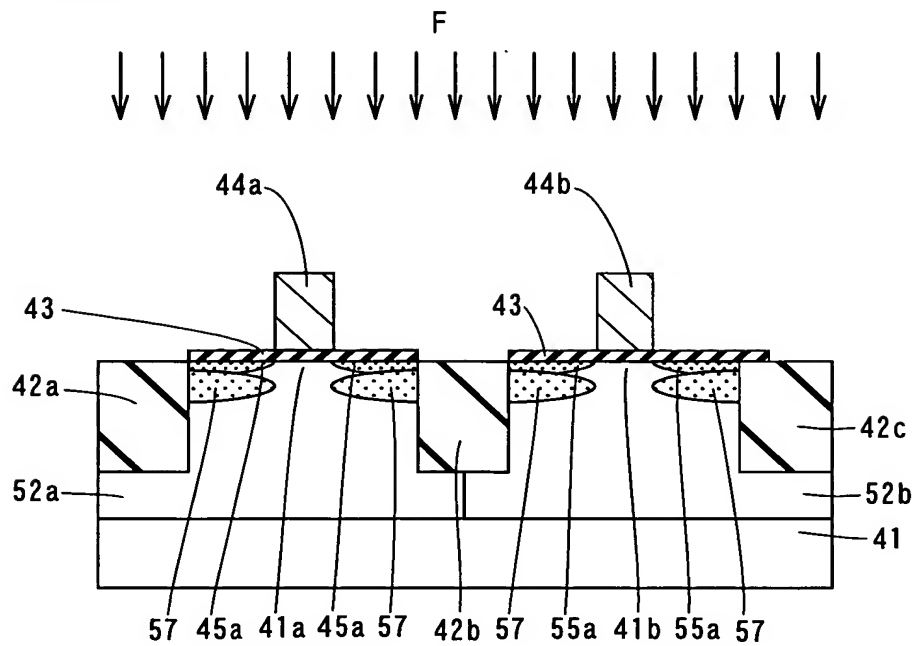
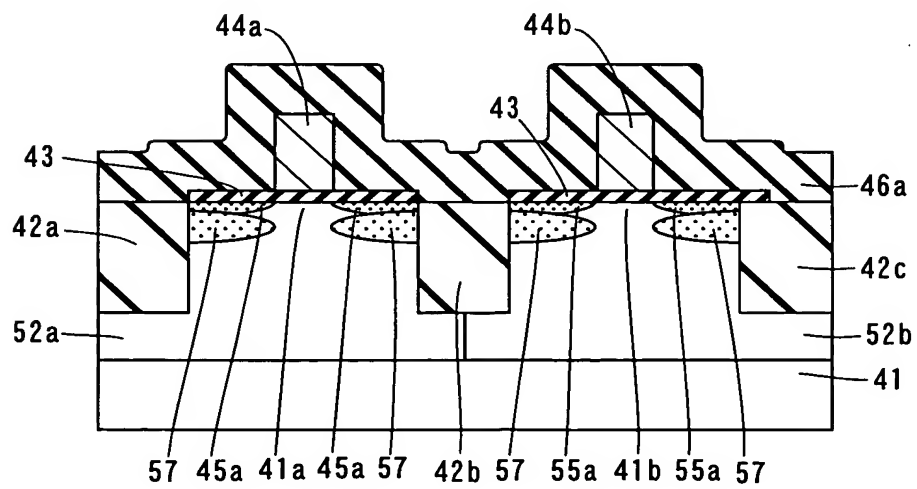


FIG.38



This diagram shows a cross-sectional view of a semiconductor device. It features a substrate 41 with a thin layer 52a on top. Two gate structures 43 are formed on the surface. Each gate structure 43 consists of a gate dielectric layer 46 and a gate electrode 44a or 44b. The gate electrode 44a is connected to a contact pad 52b. The gate electrode 44b is connected to a contact pad 52c. The gate structures 43 are separated by a channel region 42b. The channel region 42b is defined by the gate structures 43 and the substrate 41. The channel region 42b is doped with impurities, as indicated by the hatched pattern. The gate structures 43 are also doped with impurities, as indicated by the hatched pattern. The gate structures 43 are formed on the substrate 41 by a process such as chemical vapor deposition or sputtering. The gate structures 43 are used to control the flow of current in the channel region 42b. The gate structures 43 are also used to define the active regions of the device. The gate structures 43 are formed on the substrate 41 by a process such as chemical vapor deposition or sputtering. The gate structures 43 are used to control the flow of current in the channel region 42b. The gate structures 43 are also used to define the active regions of the device.

This cross-sectional view shows a semiconductor device with a substrate 41. A layer 52a is formed on the substrate. Two raised regions, 42a and 42b, are formed on the layer 52a. Each raised region contains a core 43 and a surrounding layer 44a (for 42a) or 44b (for 42b). A layer 46 is formed on top of the raised regions. A layer 47 is formed on the surface of the substrate 41. The device is divided into regions 57, 45a, 41a, 45a, 57, 42b, 57, 55a, 41b, 55a, and 57.

A cross-sectional view of a semiconductor device. At the top, a layer labeled 'As' is shown with downward-pointing arrows indicating an applied electric field. Below this, two transistors are depicted. The left transistor has a gate stack (46) on top of a gate oxide (44a), with a channel region (43) and source/drain regions (42a, 42b). The right transistor has a gate stack (46) on top of a gate oxide (44b), with a channel region (43) and source/drain regions (42c, 42d). The device is built on a substrate (41) with a buried layer (52a). Various other regions are labeled with numbers 45a, 45b, 47, 55a, 57, and 58a.

FIG.43

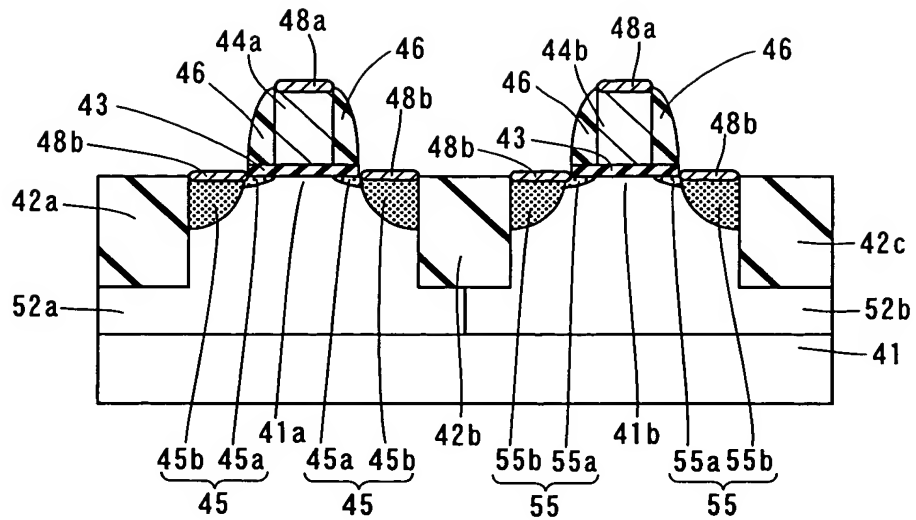


FIG.44

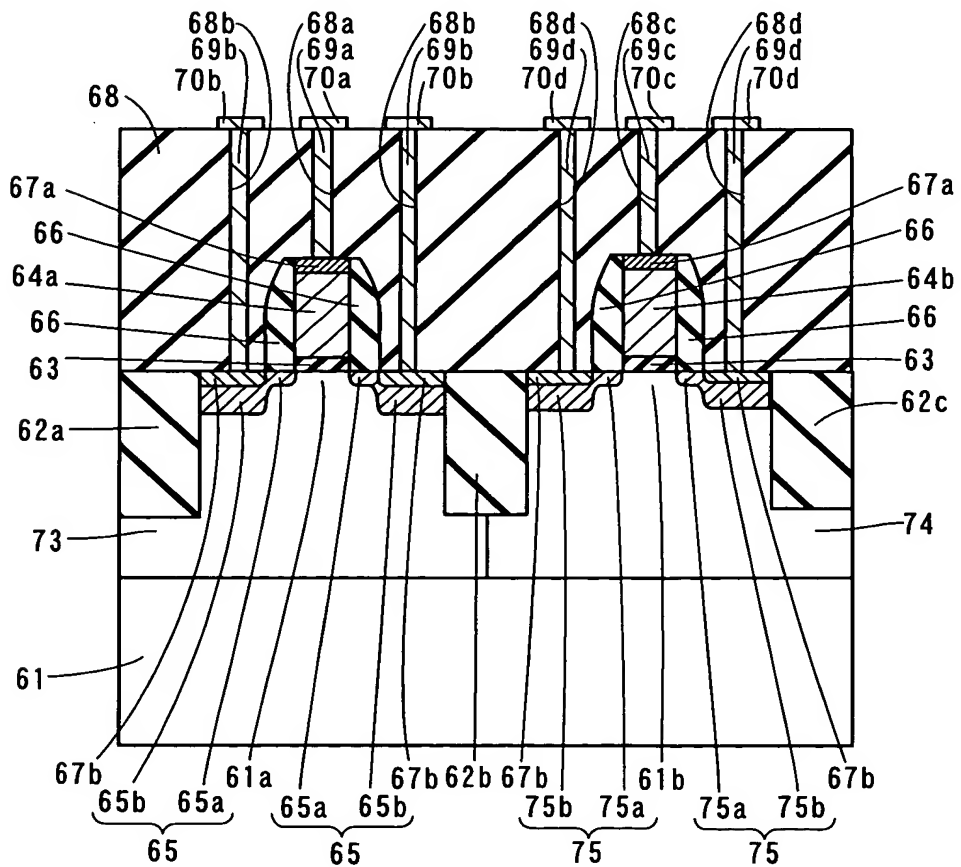


FIG.45

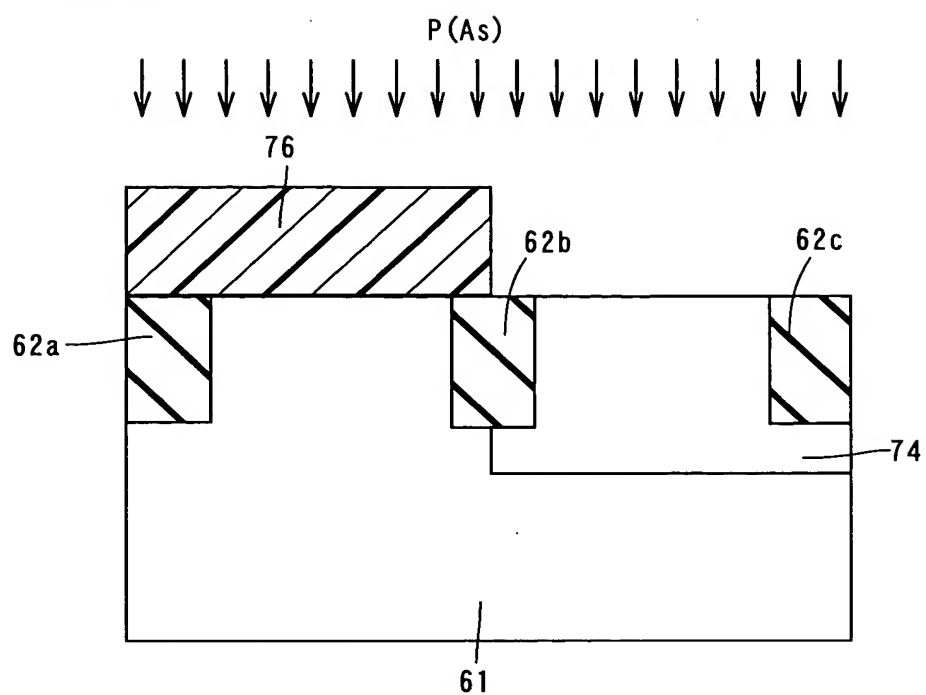


FIG.46

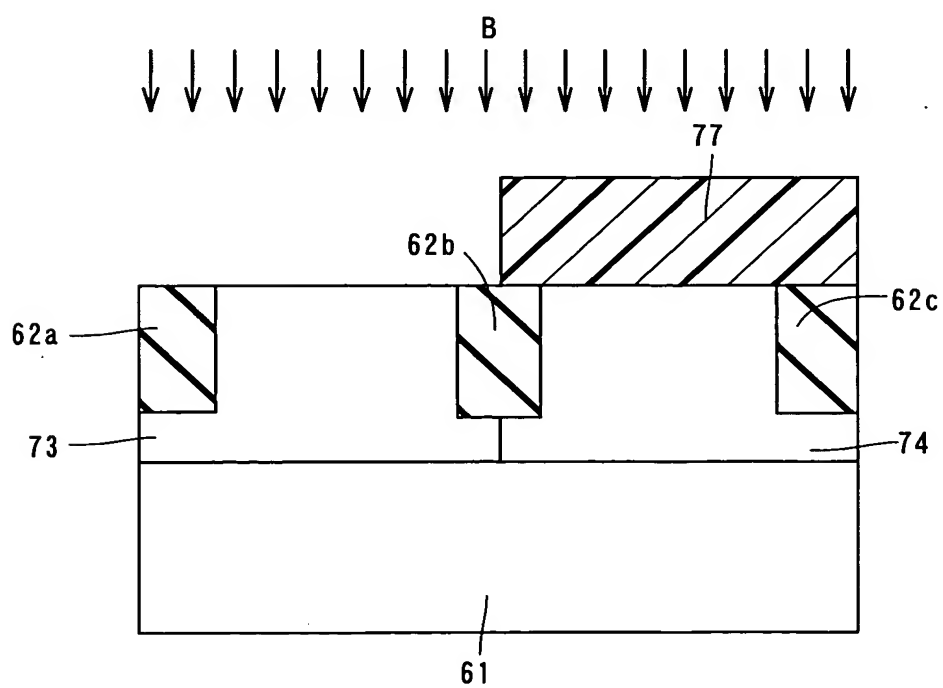


Fig. 1 is a cross-sectional view of a semiconductor device. It shows a substrate 61 with a layer 73 and 74. A central opening 62b is flanked by regions 62a and 62c. Small rectangular features 64a and 64b are positioned on top of the structure, with labels 63 pointing to the top surface of the substrate.

[illegible]

[illegible]

FIG.51

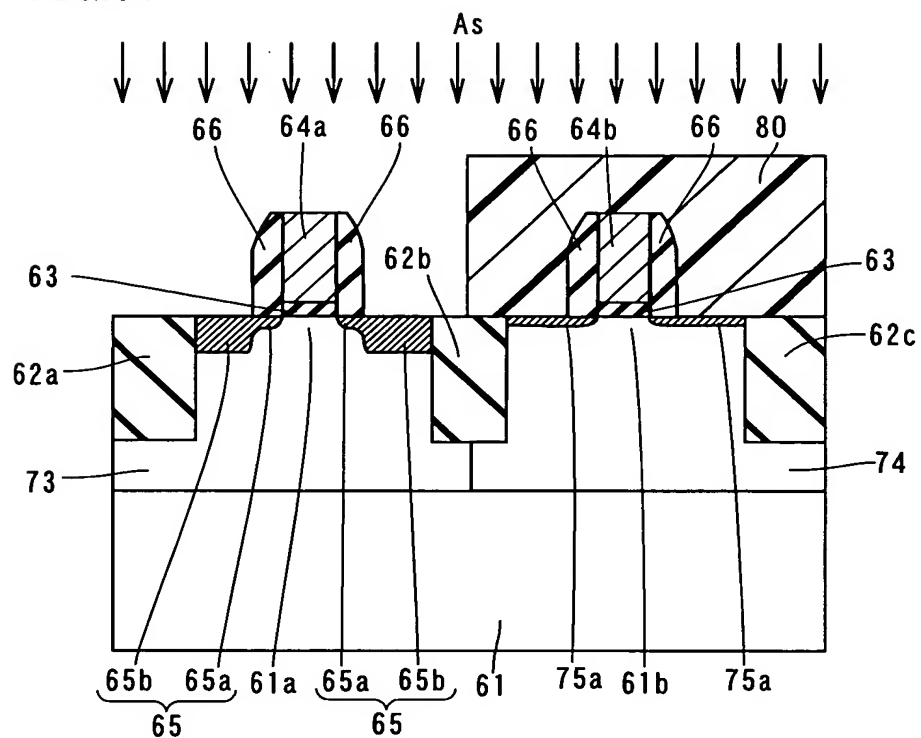


FIG.52

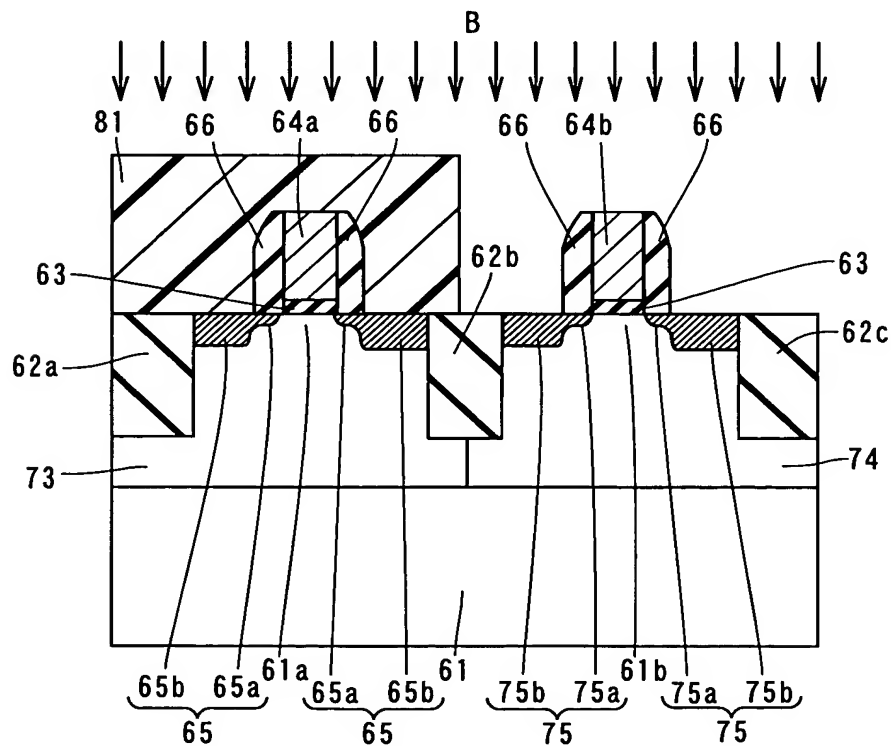


FIG.53

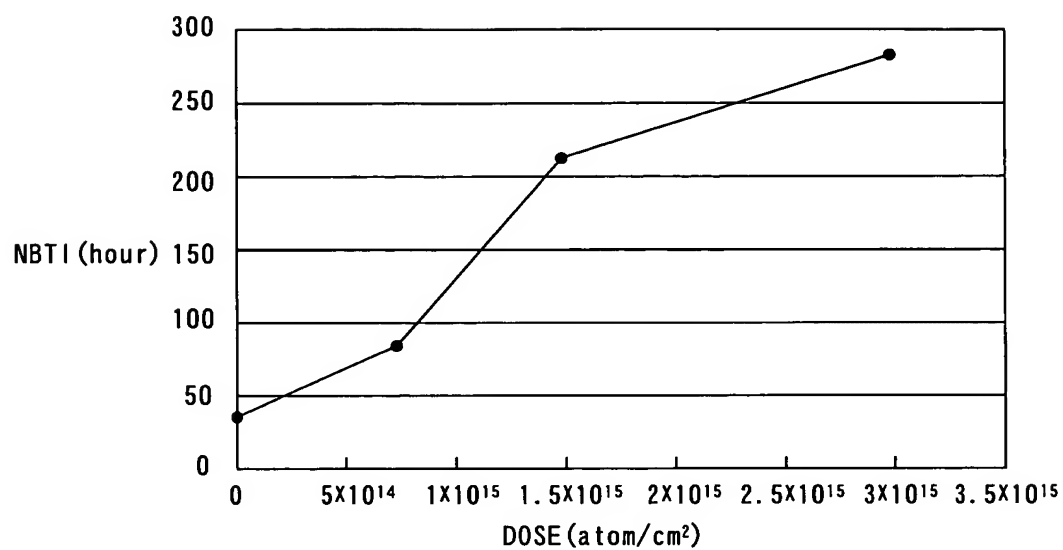


FIG.54

